

PATENT APPLICATION  
DOCKET NO.: 200209280-1

LISTING OF THE CLAIMS PER 37 C.F.R. §1.121

1. (Currently Amended) A system for generating a test case operable to test a circuit design using a plurality of threads, comprising:

a test code and state initialization engine operating responsive to a random number sequence and a probability profile for generating test code;

a distribution settings engine for generating default distribution settings that specify a magnitude of at least one simulation parameter assigned to each of said plurality of threads based on a default probability distribution profile; and

a knob-setting interface for ~~optionally~~ differentiating said default distribution settings,

wherein said ~~optionally~~ differentiated distribution settings are associated with said test code in order to generate said test case for exercising a circuit design model of said circuit design.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

2. (Currently Amended) The system as recited in claim 1, wherein said ~~optionally~~ differentiated distribution settings comprise settings that specify on a thread-by-thread basis a magnitude of at least one simulation parameter based on a user-defined probabilistic distribution profile.

3. (Original) The system as recited in claim 1, wherein said at least one simulation parameter is selected from a group of parametric variables consisting of number of instructions, loading operations, storing operations, arithmetic operations, and floating-point operations.

4. (Original) The system as recited in claim 1, wherein said test case is operable to exercise said circuit design model with events selected from the group consisting of loading operations, storing operations, arithmetic operations, and floating-point operations.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

5. (Original) The system as recited in claim 1, wherein said circuit design model comprises a multiprocessor core model.

6. (Original) The system as recited in claim 1, wherein said circuit design model comprises a register-transfer level (RTL) model of an integrated circuit.

7. (Original) The system as recited in claim 1, wherein said circuit design model comprises an architectural simulation model of an integrated circuit.

8. (Original) The system as recited in claim 1, wherein said knob-setting interface is operable to be utilized by a logical entity selected from the group consisting of a programmer, a group of programmers, and an expert system.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

9. (Original) The system as recited in claim 1, wherein said knob-setting interface comprises a Graphical User Interface (GUI).

10. (Original) The system as recited in claim 1, wherein said distribution settings engine is implemented in a software language selected from the group consisting of C, C++, and Perl.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

11. (Currently Amended) A method for generating a test case operable to test a circuit design using a plurality of threads, comprising:

generating test code including state initializations;

building default distribution settings for said multiple threads;

~~optionally~~ differentiating said default distribution settings, on a thread-by-thread basis, using a knob-setting interface;

building at least one thread-specific distribution setting, wherein said default distribution settings with respect to a specific thread are overridden; and

associating said default and thread-specific distribution settings with said test code, thereby generating a test case for exercising a circuit design model of said circuit design.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

12. (Original) The method as recited in claim 11, wherein the operation of generating test code comprises generating test code including state initializations based upon a random number sequence supplied by a random number generator.

13. (Original) The method as recited in claim 11, wherein the operation of generating test code comprises generating test code including state initializations based upon a probability profile supplied by an event probability generator.

14. (Original) The method as recited in claim 11, wherein the operation of building default distribution settings comprises assigning a magnitude of at least one simulation parameter for each of said plurality of threads based on a default probability distribution profile.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

15. (Original) The method as recited in claim 14, further comprising selecting said at least one simulation parameter from a group of parametric variables consisting of number of instructions, loading operations, storing operations, arithmetic operations, and floating-point operations.

16. (Original) The method as recited in claim 11, wherein the operation of ~~optionally~~ differentiating said distribution settings comprises providing thread-specific distribution settings via a Graphical User Interface (GUI) that operates as said knob-setting interface.

17. (Original) The method as recited in claim 11, wherein the operation of building at least one thread-specific distribution setting further comprises specifying on a thread-by-thread basis a magnitude of at least one simulation parameter based on a user-defined probabilistic distribution profile.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

18. (Currently Amended) A computer-readable medium operable with a computer platform to generate a test case for testing a circuit design using a plurality of threads, the medium having stored thereon:

instructions for generating test code including state initializations;

instructions for building default distribution settings for said multiple threads;

instructions for presenting a knob-setting interface that enables ~~optional~~ differentiation of said default distribution settings;

instructions for overriding said default distribution settings with at least one thread-specific distribution setting generated via said knob-setting interface; and

instructions for associating said default and thread-specific distribution settings with said test code, thereby generating a test case for executing a circuit design model of said circuit design.



PATENT APPLICATION  
DOCKET NO.: 200209280-1

19. (Original) The computer-readable medium as recited in claim 18, wherein said instructions for generating test code comprises instructions for generating test code including state initializations based upon a random number sequence supplied by a random number generator.

20. (Original) The computer-readable medium as recited in claim 18, wherein said instructions for generating test code comprises instructions for generating test code including state initializations based upon a probability profile supplied by an event probability generator.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

21. (Original) The computer-readable medium as recited in claim 18, wherein said instructions for building default distribution settings comprises instructions for assigning a number of commands for each of said plurality of threads based on a default probability distribution profile.

22. (Original) The computer-readable medium as recited in claim 18, wherein said instructions for presenting a knob-setting interface comprise instructions for providing a user a Graphical User Interface (GUI) that enables inputting of thread-specific knob settings.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

23. (Currently Amended) A system for generating a test case operable to test a circuit design using a plurality of threads, comprising:

means for generating test code including state initializations;

means for building default distribution settings for said multiple threads;

means for ~~optionally~~ differentiating said default distribution settings on a thread-by-thread basis;

means for building at least one thread-specific distribution setting, wherein said default distribution settings with respect to a specific thread are overridden; and

means for associating said default and thread-specific distribution settings with said test code, thereby generating a test case for exercising a circuit design model of said circuit design.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

24. (Original) The system as recited in claim 23, wherein said means for generating test code comprises means for generating test code including state initializations based upon a random number sequence supplied by a random number generator.

25. (Original) The system as recited in claim 23, wherein said means for generating test code comprises means for generating test code including state initializations based upon a probability profile supplied by an event probability generator.

26. (Original) The system as recited in claim 23, wherein said means for building default distribution settings comprises means for assigning a magnitude of at least one simulation parameter for each of said plurality of threads based on a default probability distribution profile.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

27. (Original) The system as recited in claim 26, wherein said at least one simulation parameter is selected from a group of parametric variables consisting of number of instructions, loading operations, storing operations, arithmetic operations, and floating-point operations.

28. (Currently Amended) The system as recited in claim 23, wherein said means for ~~optionally~~ differentiating said distribution settings comprises means for providing thread-specific distribution settings via a Graphical User Interface (GUI) that operates as a knob-setting interface.

29. (Original) The system as recited in claim 23, wherein said means for building at least one thread-specific distribution setting comprises means for specifying on a thread-by-thread basis a magnitude of at least one simulation parameters based on a user-defined probabilistic distribution profile.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

30. (Currently Amended) A computer system operable to simulate a platform for testing a circuit design using multiple threads, the computer system comprising:

a random number generator, operating responsive to a seed, for generating a random number sequence;

an event probability generator, operating responsive to profile settings, for generating a probability profile;

a test generator for generating default distribution settings that specify a magnitude of at least one simulation parameter for each of said multiple threads based on a default probability distribution profile; and

a knob-setting interface for ~~optionally~~ differentiating said default distribution settings,

wherein said test generator generates a test case based upon said random number sequence, said probability profile, and said ~~optionally~~ differentiated distribution settings, said test case for exercising a circuit design model of said circuit design.

PATENT APPLICATION  
DOCKET NO.: 200209280-1

31. (Original) The computer system as recited in claim 30, wherein said knob-setting interface comprises a Graphical User Interface (GUI).

32. (Original) The computer system as recited in claim 30, wherein said circuit design model comprises a register-transfer level (RTL) model of an integrated circuit.

33. (Original) The computer system as recited in claim 30, wherein said circuit design model comprises an architectural simulation model of an integrated circuit.

34. (Original) The computer system as recited in claim 30, wherein said test generator is implemented in a software language selected from the group consisting of C, C++, and Perl.